Siddharth Jain

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Education

IIT HYDERABAD
PhD Student, Department of CSE
Jul 2023-Present Hyderabad, India
- Research Area: Machine Learning based Compiler Optimizations, High Performance Computing, MLIR/LLVM

IIT HYDERABAD
MTech RA in CSE
Sep 2020-Jun 2023 Hyderabad, India
- Research Assistant in Compilers Lab IITH (CGPA: 9.57/10)
- Thesis Title: *Experiments with RL4ReAl: Benchmarking and Compile-Time Improvements*

IIIT VADODARA
BTech in CSE
Jul 2015-May 2019 Gandhinagar, India
Graduated with Distinction (CGPA: 8.79/10)

Coursework

GRADUATE
Compiler Engineering
Advanced Compiler Optimizations
Compilers for Machine Learning
Program Analysis and Optimization
Deep Learning for Computer Vision
Information Retrieval

Skills

PROGRAMMING
C/C++ • Python • HTML/CSS • JavaScript • SQL

MISCELLANEOUS
Shell • LaTeX • Git • LLVM

Honors

PMRF FELLOWSHIP
Received prestigious Prime Minister's Research Fellowship - 2023

Conference Grant
Received a travel grant to attend the EuroLLVM'23 conference at Glasgow, Scotland.

Experience

SOFTWARE DEVELOPER
MaximL Labs
June 2019 – Sep 2020 Chennai, India
Worked on developing software solutions to digitalize planning and monitoring of turnarounds operations in large-scale industries

SOFTWARE DEVELOPER INTERN
MaximL Labs
Jan 2019 – May 2019 Chennai, India
Worked on developing algorithmic solutions for resource-leveling problem in turnarounds operations in large-scale industries

RESEARCH INTERN
IRLP Lab, DAIICT
May 2018 – Juy 2018 Gandhinagar, India
Worked on extraction and summarization of patients' data from the medical reports using NLP techniques

Publications

CONFERENCES
RL4ReAl: Reinforcement Learning for Register Allocation (Link)
Published Feb 2023 ACM SIGPLAN CC 2023
- Authors: S. VenkataKeerthy, **Siddharth Jain**, Anilava Kundu, Rohit Aggarwal, Albert Cohen, and Ramakrishna Upadrasta

WORKSHOPS
ML-LLVM-Tools: Towards Seamless Integration of Machine Learning in Compiler Optimizations (Link)
Published May 2023 EuroLLVM Developers Meeting 2023
- Authors: **Siddharth Jain**, S. VenkataKeerthy, Umesh Kalvakuntla, Albert Cohen, and Ramakrishna Upadrasta

Recent Projects

ML-LLVM-TOOLS
IIT Hyderabad
Dec 2022 – present Hyderabad, India
A framework to integrate Machine Learning (ML) models into a open-source compiler LLVM. Developed a framework to integrate ML models developed in Python environment into LLVM Compiler Infrastructure implemented in C++.

RL4REAL
IIT Hyderabad
Aug 2021 – Dec 2022 Hyderabad, India
A Reinforcement Learning (RL) based Register Allocator for LLVM compiler. Developed a hierarchical RL based model to solve register allocation problem modeled as graph coloring for LLVM compiler.

ADVERSARIES@IR
IIT Hyderabad
Sep 2020 – Dec 2020 Hyderabad, India
An adversarial example generator for IR2Vec (code embedding generator) based code classifier. Developed a technique to generate adversarial examples for IR2Vec based code classifier using gradient-based methods.